

October 2003 SPS Ion Beam Test: Desiderata

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1. Introduction

The AMS RICH collaboration reserved a time window at CERN SPS from October 8 to October 19, 2003. The beam of 158 GeV/A Indium ($Z = 49$) ions will allow a better determination of the RICH charge resolution for $Z > 25$ (in addition to the $Z < 25$ range already studied in 2002).

Tracker and TOF are invited to participate as “guest” devices (like during the 2002 test): their DAQ setups must be independent; the event ID provided by the RICH will be the only way to correlate their measurements.

2. TOF test: desiderata

The next ion beam test will be the only possibility to test the scintillator FE electronics before the production and integration phases foreseen in 2004. In particular, it is important to test the charge measurement with SFET2 and SFEC2 prototypes, and the DAQ chain in the S-crate using a SDR2 prototype to read SFEx2.

Things needed in the beam area (figure 1):

- 1 SFET2 EM/QM;
- 1 SDR2 EM/QM or Altera based board;
- 1 SFEC2 EM;
- 1 custom backplane or mechanical support + point-to-point connections;
- 1 custom trigger board (TB, based on a Guido board).

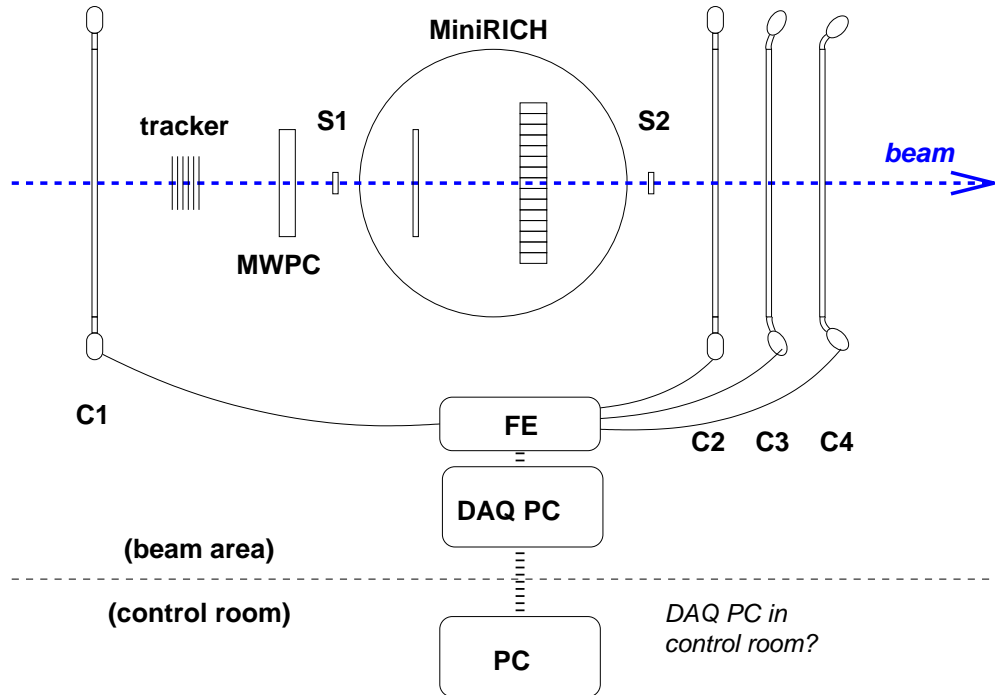


Figure 1. Proposed setup for the TOF DAQ during the SPS beam test on October 2003. A single PC (the DAQ PC) could be used instead of two computers if a reliable communication between FE in the beam area and the control room is feasible.

Up to four TOF counter C1 ... C4 can be read by 1 SFET2 (8 channels), and a single Pouxé's chip (16 ch.) of the SFEC2 is sufficient to read all dynodes. C1 and C2 will be straight counters, whereas C3 and C4 will have curved light guides.

The FT has to be generated locally, by the custom trigger board (TB). The TB will read the 8 HT and 8 SHT TTL outputs from the SFET2 and will produce a FT when the following condition is met (C_i is the AND of the HT of the two sides of counter C_i):

$$FT = C1 \cdot C2 \cdot C3 + C1 \cdot C3 \cdot C4$$

(in this way absolute trigger efficiency of C4 and C2 can be determined). The FT must be sent to SFET2 as LVDS signal and to SDR2 & SFEC2 as TTL signal. All FT signals are sent via backplane.

In addition, the TB must send the following informations to the SDR prototype:

- 8 HT pattern and scalers;
- 8 SHT pattern and scalers;

- 1 TB = trigger bit (TB = 0 when FT = C1 · C2 · C3, TB = 1 when FT = C1 · C3 · C4)

The SDR2 will read SFEx2 and TB data via point-to-point connections (TOFwire protocol) and will receive the LVL1 trigger via LVDS signal on front panel connector. On the same connector (but different pins) the board will send the system BUSY as LVDS signal.

Finally, a 24-bit event number is supposed to come from the RICH DAQ setup via LVDS twisted pairs. Two other twisted pairs of the same bundle are used to receive the general trigger (GT) and to send the TOF veto (TV) to the RICH setup.

The FT produced by the TB will be combined with the general trigger (GT = S1 · S2) to form the LVL1 trigger:

$$\text{LVL1} = \text{FT} \cdot \text{GT} \cdot (\text{no SDR BUSY}) .$$

There are two possibilities:

1. The SDR prototype is based on Altera and there is space on this PAL to manage the LVL1 production and event ID recording. The TOF veto is the only output line that must be sent to the RICH setup (via LVDS lines, in the same bundle that carries the event ID and GT). The SDR communication with the DAQ PC is to be fixed (parallel port?).
2. The SDR is Actel based (SDR2 EM). The LVL1 and TOF veto production and the event ID recording can be done by the TB. In this case the TB must receive also the SDR2 BUSY (same connector as LVL1, transmitted from TB to SDR2). The SDR2 communication with the DAQ PC is through AMSwire (the PC needs a AMSwire/PCI or parallel port interface). The LVL1 signal must be sent also to a scaler.

3. Counters, cables, electronics

- 4 complete TOF counters (light tight, if possible) with flight cables and savers;
- 5–8 m LEMO cables (for anodes) and twisted pairs (for dynodes) connecting counters to the FE crate;
- FE crate: custom backplane (or mechanical support + point-to-point connections) + SFET2 + SDR2 + SFEC2 + custom trigger board;
- LV power supplies: ± 5.6 V, 3.3 V, 5 V;

- 40–50 m twisted pair bundles connecting FE crate with RICH DAQ station (min. 26 lines for event ID, GT, TV);
- 40–50 m HV coaxial cables (about 20 cables, min. 16) for PMT powering;
- HV power supplies (3 kV, 20 ch.);
- DAQ station: 1 PC with AMSwire2PCI (or parallel port) interface if we have the SDR2 EM;
- ...